Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.- 31. (CANCELED)

32. (currently amended) A method for reducing distortion of a signal applied to an input of a high frequency circuit having a parasitic capacitance between said input and ground, comprising the steps of:

employing a device responsive to a rate of change of voltage for detecting at said input a direction of change in voltage of said input signal;

activating a charge pump for introducing a current to said parasitic capacitance to prevent said parasitic capacitance from drawing current from said input signal responsive to detection of a rate of change of a positive edge of said input signal by said device; ~~and~~

said charge pump having a first transistor which is activated for preventing discharge of said parasitic capacitance into the input of the circuit by preventing a change of voltage at said input responsive to detection of a rate of change of a negative edge of said input signal;

further comprising:

the first transistor connected to a first node, a second node, and a third node;

a second transistor connected to the first node and the second node;

a third transistor connected to the second node, a fourth node, and ground;

a fourth transistor connected to the fourth node and ground;

a current source connected to the first node and the fourth node; and

a capacitor connected to a fifth node and the fourth node.

33. (CANCELED)

34. (currently amended) An apparatus for reducing distortion of a signal applied to an input of a circuit operating at a high frequency and having a parasitic capacitance between said input and ground, comprising:

a rate of change of voltage detection circuit coupled to said input for detecting a change in voltage of said input signal;

a correction circuit comprising a charge pump circuit coupled between said detection circuit and said input to generate a current for compensating for current from said input signal diverted to said parasitic capacitance responsive to a rate of

change of voltage of a positive edge of said input signal detected by said detection circuit;

said detection circuit comprises a capacitor coupled between a common terminal and said input;

said charge pump having a first transistor which is activated for preventing discharge of said parasitic capacitance into the input of said circuit operating at a high frequency by preventing a change of voltage at said input responsive to detection of a rate of change of a negative edge of said input signal;

~~furtherer~~ further comprising:

the first transistor is connected to a first node, a second node, and a third node;

a second transistor is connected to the first node and the second node;

a third transistor is connected to the second node, the common terminal, and ground;

a fourth transistor is connected to the common terminal and ground;

and

a current source is connected to the first node and the common terminal.

35. (CANCELED)

36. (CANCELED)

37. (CANCELED)

38. (previously presented) The apparatus of claim 34 wherein said detection circuit being isolated from an output of the circuit operating at a high frequency.

39. (CANCELED)

40. (CANCELED)

41. (currently amended) The method of claim [[40]] 32, wherein:

the first transistor is a PMOS transistor;

the second transistor is a PMOS transistor;

the third transistor is an NMOS transistor; and

the fourth transistor is an NMOS transistor.

42. (currently amended) The apparatus of claim 34, wherein:

the first transistor is a PMOS transistor;

the second transistor is a PMOS transistor;

the third transistor is [[a]]an NMOS transistor; and

the fourth transistor is [[a]]an NMOS transistor.

43. (previously presented) An apparatus for reducing distortion of a signal applied to an input of a circuit operating at a high frequency and having a parasitic capacitance between said input and ground, comprising:

a rate of change of voltage detection circuit coupled to said input for detecting a change in voltage of said input signal;

a correction circuit comprising a charge pump circuit coupled between said detection circuit and said input wherein the correction circuit compensates for variations of said input signal caused by said parasitic capacitance;

said detection circuit comprises a capacitor coupled between a common terminal and said input; and

wherein the high frequency circuit comprises:

a first transistor coupled to a first node, a second node, and a third node;

a second transistor coupled to the first node and the second node;

a third transistor coupled to the second node, the common terminal, and ground;

a fourth transistor coupled to the common terminal and ground; and

a current source coupled to the first node and the common terminal.

44. (currently amended) The apparatus of claim 43, wherein:

the first transistor is a PMOS transistor;

the second transistor is a PMOS transistor;

the third transistor is [[a]]an NMOS transistor; and

the fourth transistor is [[a]]an NMOS transistor.